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Refine Search:	(19	or 15	or	11	or 12	? or	14)	and	116	

Search History

DB Name	<u>Query</u>	Hit Count	Set Name
JPAB,EPAB,DWPI	(19 or 15 or 11 or 12 or 14) and 116	14	<u>L20</u>
JPAB,EPAB,DWPI	(13 or 15 or 11 or 12 or 14) and 116	25	<u>L19</u>
JPAB,EPAB,DWPI	(13 or 15) and (11 or 12 or 14) and 116	4	<u>L18</u>
JPAB,EPAB,DWPI	(13 or 15) and (11 or 12 or 14)	71	<u>L17</u>
JPAB,EPAB,DWPI	112 and 111 and (110 or 18 or 17)	28	<u>L16</u>
JPAB,EPAB,DWPI	112 and 111 and 110 and (18 or 17)	3	<u>L15</u>
JPAB,EPAB,DWPI	112 and 111 and 110 and 18 and 17	0	<u>L14</u>
JPAB,EPAB,DWPI	synchronous and memory and controller and timing and edge and phase	1	<u>L13</u>
JPAB,EPAB,DWPI	synchronous same memory	5322	<u>L12</u>
JPAB,EPAB,DWPI	memory same controller	60903	<u>L11</u>
JPAB,EPAB,DWPI	phase same (comparing or shift or detector or decoder)	83804	<u>L10</u>
JPAB,EPAB,DWPI	phase adj (comparing or shift or detector or decoder)	42720	<u>L9</u>
JPAB,EPAB,DWPI	timing same difference	9457	<u>L8</u>
JPAB,EPAB,DWPI	leading same edge	41715	<u>L7</u>
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JPAB,EPAB,DWPI	leading edge	30666	<u>L5</u>
JPAB,EPAB,DWPI	timing difference	483	<u>L4</u>
JPAB,EPAB,DWPI	phase and (comparing or shift or detector or decoder)	95273	L3

JPAB,EPAB,DWPI	phase and (comparing or shift or detector or decoder)	95273	т э
JPAB,EPAB,DWPI	,	93213	<u>L3</u>
	memory controller	6798	<u>L2</u>
JPAB,EPAB,DWPI	synchronous memory	221	<u>L1</u>

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Search Results - Record(s) 1 through 4 of 4 returned.

1. Document ID: JP 57204407 A

Entry 1 of 4

File: JPAB

Dec 15, 1982

PUB-NO: JP357204407A

DOCUMENT-IDENTIFIER: JP 57204407 A

TITLE: ULTRASONIC THICKNESS MEASURING DEVICE OF TOOTH

Full Title Citation Front Review Classification Date Reference Claims KWIC Clip Img Image

2. Document ID: US 3810385 A

Entry 2 of 4

File: EPAB

May 14, 1974

PUB-NO: US003810385A

DOCUMENT-IDENTIFIER: US 3810385 A

TITLE: TRANSDUCER MEANS FOR ULTRASONIC EXTENSOMETER

Full Title Citation Front Review Classification Date Reference Claims KWC Image

3. Document ID: US 3759090 A

Entry 3 of 4

File: EPAB

Sep 18, 1973

PUB-NO: US003759090A

DOCUMENT-IDENTIFIER: US 3759090 A TITLE: ULTRASONIC EXTENSOMETER

Full Title Citation Front Review Classification Date Reference Claims KMC Image

4. Document ID: SU 763907 B

Entry 4 of 4

File: DWPI

Sep 18, 1980

DERWENT-ACC-NO: 1981-G2278D

DERWENT-WEEK: 198127

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TITLE: <u>Echo</u>-method flaw detection slide rule - has cursor moving along body section having logarithmic scales enabling calculation of flaw diameter

Full Title Citation Front Review Classification Date Reference Claims KMC Image

Term	Documents
VERNIER.DWPI,EPAB,JPAB.	2084
VERNIERS.DWPI,EPAB,JPAB.	103
ECHO.DWPI,EPAB,JPAB.	20106
ECHOES.DWPI,EPAB,JPAB.	3562
ECHOS.DWPI,EPAB,JPAB.	· 480
ECHOE.DWPI,EPAB,JPAB.	21
(VERNIER AND ECHO).JPAB,EPAB,DWPI.	4

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Search Results - Record(s) 1 through 1 of 1 returned.

Document ID: DE 4001533 A, GB 2228645 A, JP 02193477 A, JP 02193478 A, JP 02203686 A, DE 4001533 C, US 5179477 A, GB 2267011 A, GB 2228645 B, GB 2267011 B, US 5486955 A
 Entry 1 of 1
 File: DWPI
 Aug 2, 1990

DERWENT-ACC-NO: 1990-240154

DERWENT-WEEK: 199630

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TITLE: VTR utilising speed-independent pseudo-vertical sync signal - substitutes demodulated signal from preceding field interval of independent third magnetic head during vacant field intervals

Full	Title	Citation	Front	Review	Classification	Date	Reference	Claims	KWIC	Image
------	-------	----------	-------	--------	----------------	------	-----------	--------	------	-------

Term	Documents
SYNCHRONOUS.DWPI,EPAB,JPAB.	71461
SYNCHRONOU.DWPI,EPAB,JPAB.	17
MEMORY.DWPI,EPAB,JPAB.	645807
MEMORIES.DWPI,EPAB,JPAB.	48650
MEMORYS.DWPI,EPAB,JPAB.	28
CONTROLLER.DWPI,EPAB,JPAB.	491777
CONTROLLERS.DWPI,EPAB,JPAB.	23522
TIMING.DWPI,EPAB,JPAB.	176659
TIMINGS.DWPI,EPAB,JPAB.	6227
EDGE.DWPI,EPAB,JPAB.	671789
(SYNCHRONOUS AND MEMORY AND CONTROLLER AND TIMING AND EDGE AND PHASE).JPAB,EPAB,DWPI.	1

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Display 10 Documents including document number 1

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Search Results - Record(s) 1 through 3 of 3 returned.

1. Document ID: JP 01160368 A

Entry 1 of 3

File: JPAB

Jun 23, 1989

PUB-NO: JP401160368A

DOCUMENT-IDENTIFIER: JP 01160368 A

TITLE: PHASE CONTROLLER OF POWER CONVERTER

Full Title Citation Front Review Classification Date Reference Claims KMC Clip Img Image

2. Document ID: US 5940344 A, JP 11120769 A

Entry 2 of 3

File: DWPI

Aug 17, 1999

DERWENT-ACC-NO: 1999-332572

DERWENT-WEEK: 199939

COPYRIGHT 1999 DERWENT INFORMATION LTD

TITLE: Synchronous semiconductor memory e.g. dynamic random-access memory (DRAM) - has phase comparator which collates timing of level variation of signals flowing

within first and second signal lines, respectively

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KMC | Image |

3. Document ID: JP 08180660 A

Entry 3 of 3

File: DWPI

Jul 12, 1996

DERWENT-ACC-NO: 1996-376493

DERWENT-WEEK: 199638

COPYRIGHT 1999 DERWENT INFORMATION LTD

TITLE: Disk recording-and-reproducing appts. for e.g. small computer - has head controller that regulates positions of magnetic heads on surface of corresp. magnetic disks based on synchronous timing signal obtd. from timing signal

generator

Full Title Citation Front Review Classification Date Reference Claims KWC Image

Term	Documents
(12 AND (8 OR 7) AND 11 AND 10).JPAB,EPAB,DWPI.	3

Display 10 Documents

including document number 3

3

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Search Results - Record(s) 1 through 10 of 28 returned.

1. Document ID: JP 07230685 A

Entry 1 of 28

File: JPAB

Aug 29, 1995

PUB-NO: JP407230685A

DOCUMENT-IDENTIFIER: JP 07230685 A

TITLE: MULTI-BANK SYNCHRONOUS MEMORY SYSTEM HAVING CASCADE TYPE MEMORY CELL

STRUCTURE

Full Title Citation Front Review Classification Date Reference Claims

Document ID: JP 10283777 A

Entry 2 of 28

File: JPAB

Oct 23, 1998

PUB-NO: JP410283777A

DOCUMENT-IDENTIFIER: JP 10283777 A

TITLE: SEMICONDUCTOR INTEGRATED CIRCUIT WHERE SDRAM CORE AND LOGIC CIRCUIT ARE

MIXEDLY MOUNTED ON SINGLE CHIP AND TESTING METHOD OF THE SDRAM CORE

Full Title Citation Front Review Classification Date Reference Claims KWC Image

3. Document ID: JP 10199239 A

Entry 3 of 28

File: JPAB

Jul 31, 1998

PUB-NO: JP410199239A

DOCUMENT-IDENTIFIER: JP 10199239 A

TITLE: SEMICONDUCTOR MEMORY DEVICE SYSTEM AND SEMICONDUCTOR MEMORY DEVICE

Full Title Citation Front Review Classification Date Reference Claims KMC ClipImg Image

Document ID: JP 09258956 A

Entry 4 of 28

File: JPAB

Oct 3, 1997

PUB-NO: JP409258956A

DOCUMENT-IDENTIFIER: JP 09258956 A

TITLE: PRINTER CONTROLLER

Title Citation Front Review Classification Date Reference Claims KWIC Clip Img Image

Document ID: JP 04360194 A

Entry 5 of 28

File: JPAB

Dec 14, 1992

PUB-NO: JP404360194A

DOCUMENT-IDENTIFIER: JP 04360194 A TITLE: DISPLAY MEMORY CONTROLLER

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KMC | Clip Img | Image

6. Document ID: JP 02164151 A

Entry 6 of 28

File: JPAB

Jun 25, 1990

PUB-NO: JP402164151A

DOCUMENT-IDENTIFIER: JP 02164151 A

TITLE: SPREAD SPECTRUM COMMUNICATION EQUIPMENT

Full Title Citation Front Review Classification Date Reference Claims KWC Clip Img Image

7. Document ID: JP 01160368 A

Entry 7 of 28

File: JPAB

Jun 23, 1989

PUB-NO: JP401160368A

DOCUMENT-IDENTIFIER: JP 01160368 A

TITLE: PHASE CONTROLLER OF POWER CONVERTER

Full Title Citation Front Review Classification Date Reference Claims KMC Clip Img Image

8. Document ID: JP 56019378 A

Entry 8 of 28

File: JPAB

Feb 24, 1981

PUB-NO: JP356019378A

DOCUMENT-IDENTIFIER: JP 56019378 A

TITLE: PHASE CONTROLLER

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KMC | Clip Img | Image |

9. Document ID: EP 312200 A2

Entry 9 of 28

File: EPAB

Apr 19, 1989

PUB-NO: EP000312200A2

DOCUMENT-IDENTIFIER: EP 312200 A2

TITLE: Synchroniser for a decoder and decoder system.

Full Title Citation Front Review Classification Date Reference Claims KMC Image

10. Document ID: JP 11161363 A

Entry 10 of 28

File: DWPI

Jun 18, 1999

DERWENT-ACC-NO: 1999-409063

DERWENT-WEEK: 199935

COPYRIGHT 1999 DERWENT INFORMATION LTD

TITLE: Internal clock generator circuit for semiconductor memory device - has controller that cuts-off clock path to phase detector from synchronous delay circuit, when concurrence of phase of external and internal clocks is detected

Full Title Citation Front Review Classification Date Reference Claims KWIC Image

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Search Results - Record(s) 11 through 20 of 28 returned.

11. Document ID: US 5940344 A, JP 11120769 A

Entry 11 of 28

File: DWPI

Aug 17, 1999

DERWENT-ACC-NO: 1999-332572

DERWENT-WEEK: 199939

COPYRIGHT 1999 DERWENT INFORMATION LTD

TITLE: Synchronous semiconductor memory e.g. dynamic random-access memory (DRAM) has phase comparator which collates timing of level variation of signals flowing within first and second signal lines, respectively

Full Title Citation Front Review Classification Date Reference Claims KWC Image

12. Document ID: JP 11110280 A

Entry 12 of 28

File: DWPI

Apr 23, 1999

DERWENT-ACC-NO: 1999-317912

DERWENT-WEEK: 199927

COPYRIGHT 1999 DERWENT INFORMATION LTD

TITLE: SDRAM semiconductor memory system for synchronous data forwarding in personal computer - detects maximum flight time of memory location addresses from where data is to be accessed serially and gives equal amount of delay to data output start clock

Full Title Citation Front Review Classification Date Reference Claims KWC Image

13. Document ID: US 5946268 A, JP 11074783 A

Entry 13 of 28

File: DWPI

Aug 31, 1999

DERWENT-ACC-NO: 1999-251152

DERWENT-WEEK: 199942

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TITLE: Internal clock signal generator for synchronous semiconductor memory includes delay controller which adjusts delay time of delay line based on phase difference between internal and external clock signal

Full Title Citation Front Review Classification Date Reference Claims KMIC Image

14. Document ID: JP 11032274 A

Entry 14 of 28

File: DWPI

Feb 2, 1999

DERWENT-ACC-NO: 1999-178038

DERWENT-WEEK: 199915

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TITLE: Memory read-write <u>controller</u> of multiscreen display device - writes video signal in predefined space of <u>memory</u> based on phase of vertical synchronizing signal and <u>memory</u> content is read according to predefined synchronizing signal

Full Title Citation Front Review Classification Date Reference Claims KWC Image

15. Document ID: TW 358264 A, GB 2320779 A, DE 19752161 A1, JP 10199239 A, US 5896347 A
Entry 15 of 28 File: DWPI May 11, 1999

DERWENT-ACC-NO: 1998-315136

DERWENT-WEEK: 199938

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TITLE: Synchronous DRAM - includes <u>phase shift</u> circuit which introduces prescribed <u>phase</u> angle between output data and <u>second</u> synchronising signal so latch pulse can immediately be generated at controller upon receiving data strobe signal

Full Title Citation Front Review Classification Date Reference Claims KMC Image

16. Document ID: JP 09147574 A

Entry 16 of 28

File: DWPI

Jun 6, 1997

DERWENT-ACC-NO: 1997-355903

DERWENT-WEEK: 199733

COPYRIGHT 1999 DERWENT INFORMATION LTD

TITLE: Solid state memory - has delay <u>controller</u> that fixes time delay of sense amplifier <u>controller</u> relative to phase <u>difference</u> between signals output from dummy <u>memory</u> cell and sense amplifier <u>controller</u>

Full Title Citation Front Review Classification Date Reference Claims KMC Image

17. Document ID: JP 09006462 A

Entry 17 of 28

File: DWPI

Jan 10, 1997

DERWENT-ACC-NO: 1997-123349

DERWENT-WEEK: 199712

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TITLE: Data processing system for computer system - has delay controller which controls delay time of variable delay unit to eliminate phase difference detected by phase detector

Full Title Citation Front Review Classification Date Reference Claims KMC Image

18. Document ID: JP 08180660 A

Entry 18 of 28

File: DWPI

Jul 12, 1996

DERWENT-ACC-NO: 1996-376493

DERWENT-WEEK: 199638

COPYRIGHT 1999 DERWENT INFORMATION LTD

TITLE: Disk recording-and-reproducing appts. for e.g. small computer - has head controller that regulates positions of magnetic heads on surface of corresp. magnetic disks based on synchronous timing signal obtd. from timing signal generator

Full Title Citation Front Review Classification Date Reference Claims KMC Image

19. Document ID: EP 219206 A, DE 3680742 G, EP 219206 B, US 4673880 A File: DWPI Entry 19 of 28

Apr 22, 1987

DERWENT-ACC-NO: 1987-110151

DERWENT-WEEK: 198716

COPYRIGHT 1999 DERWENT INFORMATION LTD

TITLE: Phase sensitive detection in multi-slice magnetic resonance imager - has control signals generated in pulse sequencer and memory circuit, applied to transmitter through frequency synthesiser controlling sync.

Title Citation Front Review Classification Date Reference Claims KMC Image

20. Document ID: SU 1777143 A2

Entry 20 of 28

File: DWPI

Nov 23, 1992

DERWENT-ACC-NO: 1993-384590

DERWENT-WEEK: 199348

COPYRIGHT 1999 DERWENT INFORMATION LTD

TITLE: Controller of DRAM for computer engineering - has first and second sync. inputs of error corrector connected to sync. data reception and outputting outputs of memory access controller

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Fuli	Title	Citation	Front	Review	Classification	Date	Reference	Claims	KUMC	Image
		· ·								

Term	Documents
((12 AND 11) AND (8 OR 7 OR 10)).JPAB,EPAB,DWPI.	28

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including document number 21

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	Documents
((12 AND 11) AND (8 OR 7 OR 10)).JPAB,EPAB,DWPI.	28

Display 10 Documents

including document number 11

Display Format: TI

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Search Results - Record(s) 21 through 28 of 28 returned.

21. Document ID: SU 1735760 A1

Entry 21 of 28

File: DWPI

May 23, 1992

DERWENT-ACC-NO: 1993-158083

DERWENT-WEEK: 199319

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TITLE: Ultrasonic assembly, automatic frequency controller - has pairs of operational amplifiers, electronic switches and resistors, and dynamic memory

Full Title Citation Front Review Classification Date Reference Claims KWIC Image

22. Document ID: DE 69031201 E, EP 420667 A, JP 03189966 A, US 5172357 A, EP 420667 A3, EP 420667 B1

Entry 22 of 28

File: DWPI

Sep 11, 1997

DERWENT-ACC-NO: 1991-096051

DERWENT-WEEK: 199742

COPYRIGHT 1999 DERWENT INFORMATION LTD

TITLE: Clock phase synchronous controller for optical disk drive - uses pulse generator with memory information and oscillator which generates reference signal with injection-synchronised controller

Full Title Citation Front Review Classification Date Reference Claims KWC Image

23. Document ID: SU 1617586 A

Entry 23 of 28

File: DWPI

Dec 30, 1990

DERWENT-ACC-NO: 1991-338506

DERWENT-WEEK: 199146

COPYRIGHT 1999 DERWENT INFORMATION LTD

TITLE: Thyristor converter phase controller - has detector integrator memory integrator resetting switch controlled switch and sync. pulse series divider

Full Title Citation Front Review Classification Date Reference Claims KMC Image

24. Document ID: GB 2227142 A, DE 3924202 A, DE 3924202 C, GB 2227142 B, JP 02186781 A. US 5065385 A

Entry 24 of 28

File: DWPI

Jul 18, 1990

DERWENT-ACC-NO: 1990-219160

DERWENT-WEEK: 199029

COPYRIGHT 1999 DERWENT INFORMATION LTD

TITLE: Time-base compensation of signals reproduced from recording medium -

effects coarse adjustment by regulating motor rotating disc and fine adjustment by writing sampled data into memory synchronously

Full Title Citation Front Review Classification Date Reference Claims KMC Image

25. Document ID: SU 1205234 A

Entry 25 of 28

File: DWPI

Jan 15, 1986

DERWENT-ACC-NO: 1986-224443

DERWENT-WEEK: 198634

COPYRIGHT 1999 DERWENT INFORMATION LTD

TITLE: Turbogenerator rotor winding fault detector - has pulse shaper, pairs of

rectifiers and distributors with peak detectors connected to comparators

Full Title Citation Front Review Classification Date Reference Claims KWC Image

26. Document ID: US 4458308 A

Entry 26 of 28

File: DWPI

Jul 3, 1984

DERWENT-ACC-NO: 1984-182694

DERWENT-WEEK: 198429

COPYRIGHT 1999 DERWENT INFORMATION LTD

TITLE: communications controller having stretched clock cycle - is microprocessor controlled and has counter which is free-running for stretched cycle and reset on

predetermined cycle

Full Title Citation Front Review Classification Date Reference Claims KMC Image

27. Document ID: DE 3229988 A, AU 8287060 A, AU 8662613 A, CA 1215446 A, CH 668036 A, DE 3229988 C2, FR 2511521 A, GB 2106275 A, GB 2106275 B, IT 1148612 B, KR 8900025 B, SE 8204659 A, US 4510570 A

Entry 27 of 28

•

File: DWPI

Mar 10, 1983

DERWENT-ACC-NO: 1983-D5091K

DERWENT-WEEK: 198311

COPYRIGHT 1999 DERWENT INFORMATION LTD

TITLE: Power press control system - uses microcomputer press drive angle of

rotation compared with that in program

Full Title Citation Front Review Classification Date Reference Claims KWC Image

28. Document ID: DD 148266 A, DD 148266 B

Entry 28 of 28

File: DWPI

May 13, 1981

DERWENT-ACC-NO: 1981-H2710D

DERWENT-WEEK: 198132

COPYRIGHT 1999 DERWENT INFORMATION LTD

TITLE: Synchronising functional units of EDP systems - using controlled and

uncontrolled timing pulses and master clocking signals

Full Title Citation Front Review Classification Date Reference Claims KMC Image

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Search Results - Record(s) 1 through 4 of 4 returned.

1. Document ID: JP 07230685 A

Entry 1 of 4

File: JPAB

Aug 29, 1995

PUB-NO: JP407230685A

DOCUMENT-IDENTIFIER: JP 07230685 A

TITLE: MULTI-BANK SYNCHRONOUS MEMORY SYSTEM HAVING CASCADE TYPE MEMORY CELL

STRUCTURE

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KMC | Clip Img | Image |

2. Document ID: JP 04360194 A

Entry 2 of 4

File: JPAB

Dec 14, 1992

PUB-NO: JP404360194A

DOCUMENT-IDENTIFIER: JP 04360194 A TITLE: DISPLAY MEMORY CONTROLLER

Full Title Citation Front Review Classification Date Reference Claims KMC Clip Img Image

3. Document ID: JP 08180660 A

Entry 3 of 4

File: DWPI

Jul 12, 1996

DERWENT-ACC-NO: 1996-376493

DERWENT-WEEK: 199638

COPYRIGHT 1999 DERWENT INFORMATION LTD

TITLE: Disk recording-and-reproducing appts. for e.g. small computer - has head controller that regulates positions of magnetic heads on surface of corresp. magnetic disks based on synchronous timing signal obtd. from timing signal

generator

Full Title Citation Front Review Classification Date Reference Claims KMC Image

4. Document ID: GB 2227142 A, DE 3924202 A, DE 3924202 C, GB 2227142 B, JP 02186781 A, US 5065385 A

Entry 4 of 4

File: DWPI

Jul 18, 1990

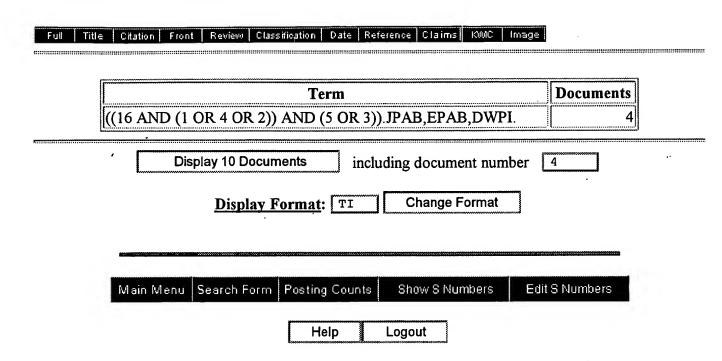
DERWENT-ACC-NO: 1990-219160

DERWENT-WEEK: 199029

COPYRIGHT 1999 DERWENT INFORMATION LTD

TITLE: Time-base compensation of signals reproduced from recording medium effects coarse adjustment by regulating motor rotating disc and fine adjustment by

writing sampled data into memory synchronously



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Search Results - Record(s) 1 through 10 of 14 returned.

1. Document ID: JP 07230685 A

Entry 1 of 14

File: JPAB

Aug 29, 1995

PUB-NO: JP407230685A

DOCUMENT-IDENTIFIER: JP 07230685 A

TITLE: MULTI-BANK SYNCHRONOUS MEMORY SYSTEM HAVING CASCADE TYPE MEMORY CELL

STRUCTURE

Full Title Citation Front Review Classification Date Reference Claims KMC ClipImg Image

Document ID: JP 10283777 A

Entry 2 of 14

File: JPAB

Oct 23, 1998

PUB-NO: JP410283777A

DOCUMENT-IDENTIFIER: JP 10283777 A

TITLE: SEMICONDUCTOR INTEGRATED CIRCUIT WHERE SDRAM CORE AND LOGIC CIRCUIT ARE

MIXEDLY MOUNTED ON SINGLE CHIP AND TESTING METHOD OF THE SDRAM CORE

Full Title Citation Front Review Classification Date Reference Claims KMC Image

3. Document ID: JP 10199239 A

Entry 3 of 14

File: JPAB

Jul 31, 1998

PUB-NO: JP410199239A

DOCUMENT-IDENTIFIER: JP 10199239 A

TITLE: SEMICONDUCTOR MEMORY DEVICE SYSTEM AND SEMICONDUCTOR MEMORY DEVICE

Full Title Citation Front Review Classification Date Reference Claims KWC ClipImg Image

Document ID: JP 04360194 A

Entry 4 of 14

File: JPAB

Dec 14, 1992

PUB-NO: JP404360194A

DOCUMENT-IDENTIFIER: JP 04360194 A TITLE: DISPLAY MEMORY CONTROLLER

Full Title Citation Front Review Classification Date Reference Claims KWC ClipImg Image

5. Document ID: JP 02164151 A

Entry 5 of 14

File: JPAB

Jun 25, 1990

PUB-NO: JP402164151A

DOCUMENT-IDENTIFIER: JP 02164151 A

TITLE: SPREAD SPECTRUM COMMUNICATION EQUIPMENT

Full Title Citation Front Review Classification Date Reference Claims KMC Clip Img Image

Document ID: JP 56019378 A

Entry 6 of 14

File: JPAB

Feb 24, 1981

PUB-NO: JP356019378A

DOCUMENT-IDENTIFIER: JP 56019378 A

TITLE: PHASE CONTROLLER

Full Title Citation Front Review Classification Date Reference Claims KMC ClipImg Image

7. Document ID: JP 11161363 A

Entry 7 of 14

File: DWPI

Jun 18, 1999

DERWENT-ACC-NO: 1999-409063

DERWENT-WEEK: 199935

COPYRIGHT 1999 DERWENT INFORMATION LTD

TITLE: Internal clock generator circuit for semiconductor memory device - has controller that cuts-off clock path to phase detector from synchronous delay circuit, when concurrence of phase of external and internal clocks is detected

Full Title Citation Front Review Classification Date Reference Claims KMC Image

8. Document ID: US 5940344 A, JP 11120769 A

Entry 8 of 14

File: DWPI

Aug 17, 1999

DERWENT-ACC-NO: 1999-332572

DERWENT-WEEK: 199939

COPYRIGHT 1999 DERWENT INFORMATION LTD

TITLE: Synchronous semiconductor memory e.g. dynamic random-access memory (DRAM) - has phase comparator which collates timing of level variation of signals flowing within first and second signal lines, respectively

Full Title Citation Front Review Classification Date Reference Claims KMC Image

9. Document ID: TW 358264 A, GB 2320779 A, DE 19752161 A1, JP 10199239 A, US 5896347 A

Entry 9 of 14 File: DWPI May 11, 1999

DERWENT-ACC-NO: 1998-315136

DERWENT-WEEK: 199938

COPYRIGHT 1999 DERWENT INFORMATION LTD

TITLE: Synchronous DRAM - includes phase shift circuit which introduces prescribed phase angle between output data and second synchronising signal so latch pulse can

immediately be generated at controller upon receiving data strobe signal

Full Title Citation Front Review Classification Date Reference Claims KMC Image

10. Document ID: JP 09006462 A

Entry 10 of 14

File: DWPI

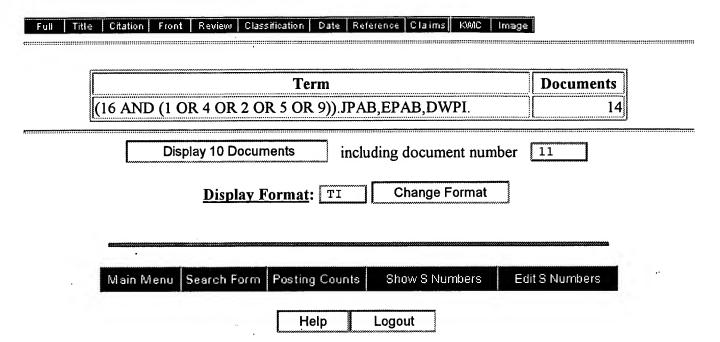
Jan 10, 1997

DERWENT-ACC-NO: 1997-123349

DERWENT-WEEK: 199712

COPYRIGHT 1999 DERWENT INFORMATION LTD

TITLE: Data processing system for computer system - has delay controller which controls delay time of variable delay unit to eliminate phase deference detected by phase detector



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Search Results - Record(s) 11 through 14 of 14 returned.

11. Document ID: JP 08180660 A

Entry 11 of 14

File: DWPI

Jul 12, 1996

DERWENT-ACC-NO: 1996-376493

DERWENT-WEEK: 199638

COPYRIGHT 1999 DERWENT INFORMATION LTD

TITLE: Disk recording-and-reproducing appts. for e.g. small computer - has head controller that regulates positions of magnetic heads on surface of corresp. magnetic disks based on synchronous timing signal obtd. from timing signal generator

Full Title Citation Front Review Classification Date Reference Claims KMC Image

12. Document ID: SU 1777143 A2

Entry 12 of 14

File: DWPI

Nov 23, 1992

DERWENT-ACC-NO: 1993-384590

DERWENT-WEEK: 199348

COPYRIGHT 1999 DERWENT INFORMATION LTD

TITLE: $\underline{\text{Controller}}$ of DRAM for computer engineering - has first and second sync. inputs of error corrector connected to sync. data reception and outputting outputs of $\underline{\text{memory}}$ access $\underline{\text{controller}}$

Full Title Citation Front Review Classification Date Reference Claims KMC Image

13. Document ID: GB 2227142 A, DE 3924202 A, DE 3924202 C, GB 2227142 B, JP 02186781 A, US 5065385 A

Entry 13 of 14

File: DWPI

Jul 18, 1990

DERWENT-ACC-NO: 1990-219160

DERWENT-WEEK: 199029

COPYRIGHT 1999 DERWENT INFORMATION LTD

TITLE: Time-base compensation of signals reproduced from recording medium - effects coarse adjustment by regulating motor rotating disc and fine adjustment by writing sampled data into memory synchronously

Full Title Citation Front Review Classification Date Reference Claims KWIC Image

14. Document ID: SU 1205234 A

Entry 14 of 14

File: DWPI

Jan 15, 1986

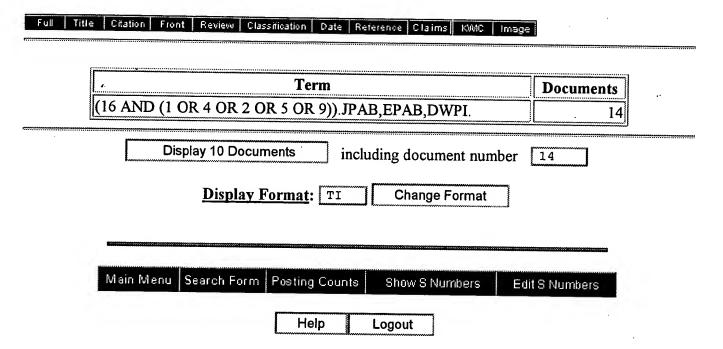
DERWENT-ACC-NO: 1986-224443

DERWENT-WEEK: 198634

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TITLE: Turbogenerator rotor winding fault detector - has pulse shaper, pairs of

rectifiers and distributors with peak detectors connected to comparators



	Туре	Hits	Search Text	DBs
1	IS&R	1115	(("711/147") or ("711/167") or ("326/93")).CCLS.	USPAT
2	IS&R	5	(("395/551") or ("395/552")).CCLS.	USPAT
3	IS&R	558	(("370/507") or ("370/503")).CCLS.	USPAT
4	IS&R	735	(("370/507") or ("370/503") or ("370/498")).CCLS.	USPAT
5	BŖS	1677	((("370/507") or (("370/503")).CCLS.)	USPAT
6	BRS	1853	((("370/507") or ("370/503") or ("370/498")).CCLS.)	USPAT
7	IS&R	36	(("5379398") or ("5369635") or ("5365228") or ("5363377") or ("5361260") or ("5357480") or ("5353429") or ("5345440") or ("5343096") or ("53333299") or ("53333293") or ("5333130") or ("5327468") or ("5327466") or ("5327425") or ("5327402") or ("5327394") or ("5327277") or ("5327394") or ("5327277") or ("5321368") or ("5315181") or ("5315181") or ("5315180") or ("5291480") or ("5289430") or ("5289050") or ("5287359") or ("5287359") or ("5287359") or ("5305320") or ("5305325")).PN.	USPAT

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	Time Stamp	Comments	Error Definition	Errors
	999/11/23 0:14			0
² 10	999/11/23 0:15			0
3 10	999/11/23 0:16			0
	999/11/23 0:16			0
	999/11/23 0:17			0
	999/11/23 0:53			0
	999/11/23 4:22			0

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	Type Hits		Search Text	DBs	
8	IS&R	29	(("5134636") or ("5130987") or ("5129069") or ("5125089") or ("5124980") or ("5122693") or ("5121390") or ("5121390") or ("5060239") or ("5060241") or ("5060239") or ("5107415") or ("5097532") or ("5097151") or ("5075575") or ("5042043") or ("5042043") or ("5047921") or ("5045725") or ("5043982") or ("5041747") or ("5040174") or ("5033001") or ("5027375") or ("5023484")).PN.	USPAT 	
9	IS&R	27	(("4977596") or ("4975911") or ("5012138") or ("5003461") or ("5001730") or ("4991169") or ("4989136") or ("4988901") or ("4975593") or ("4973863") or ("4970405") or ("4965811") or	USPAT	
10	, IS&R	33	(("4897836") or ("4897659") or ("4891808") or ("4884285") or ("4881223") or ("4879712") or ("4879481") or ("4878217") or ("4873663") or ("4866608") or ("4866310") or ("4866306") or ("4864556") or ("4862411") or ("4860285") or ("4847867") or	USPAT	

	Time Stamp	Comments	Error Definition	Errors
8	1999/11/23 14:30			0
9	1999/11/23 14:32			0
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10	1999/11/23 14:32			0
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	Туре	Hits _.	Search Text	DBs
11	, IS&R	32	(("4794596") or ("4786829") or ("4783633") or ("4782481") or ("4780883") or ("4779093") or ("4779009") or ("4771423") or ("4771400") or ("4771335") or ("4761799") or ("4760442") or ("4760291") or ("4757521") or ("4757469") or ("4754454") or ("4754173") or ("4740961") or ("4742252") or ("4740961") or ("4739473") or ("4736336") or ("4720828") or ("4716317") or ("4713564") or ("4700088")).PN.	USPAT
12		34	(("4694291") or ("4691294") or ("4688212") or ("4677617") or ("4675861") or ("4675811") or ("4665327") or ("4663545") or ("4658356") or ("4680779") or ("4682327") or ("4680779") or ("4683551") or ("4631718") or ("4631659") or ("4628493") or ("4628216") or ("4628493") or ("4625127") or ("4615029") or ("4597076") or ("4596025") or ("4592050") or ("4574376") or ("4532625") or ("4532625") or ("4530091") or ("45788903") or ("4575815") or ("4525832")).PN.	USPAT

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•	11	1999/11/23 14:33			0
•	12	1999/11/23 14:34			0

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	Туре	Hits	Search Text	DBs
13	., IS&R	35	(("4523104") or ("4520458") or ("4514840") or ("4509121") or ("4500992") or ("4494215") or ("4491909") or ("4484142") or ("4479065") or ("4410946") or ("4406007") or ("4477738") or ("4398103") or ("4477738") or ("4439857") or ("4438520") or ("4423507") or ("4419592") or ("4415818") or ("4392132") or ("4392065") or ("4389722") or ("4386426") or ("4383314") or ("4386295") or ("4366573") or ("4366540") or ("4357701") or ("4355386") or ("4352179") or ("4347602") or ("4345309") or ("4344121")).PN.	USPAT
14	IS&R	29	(("4287593") or ("4287589") or ("4271483") or ("4253181") or ("4314109") or ("4310921") or ("4302836") or ("4298956") or ("4288860") or ("4253146") or ("4253144") or ("4239934") or ("4229816") or	 USPAT
15	IS&R	35	(("4089052") or ("4088831") or ("4086429") or ("4074080") or ("4074073") or ("4071887") or ("4064486") or ("4061975") or ("4060794") or ("4035580") or ("4031471") or ("4023145") or ("4006314") or ("4004095") or ("4002839") or ("3993870") or ("3988597") or ("3984641") or ("3941930") or ("3967058") or ("3932841") or ("3920915") or ("3913018") or ("3911218") or ("3851252") or ("3851102") or ("3824349") or ("3818242") or ("3813526")).PN.	USPAT

	Time Stamp	Comments	Error Definition	Errors
13	1999/11/23 14:35			0
14	1999/11/23 14:35			0
15	1999/11/23 14:36			O

	Туре	Hits	Search Text	DBs
16	IŚ&R	16	(("5276858") or ("5276856") or ("5274628") or ("5268937") or ("5267240") or ("5267240") or ("5264746") or ("5263150") or ("5263027") or ("5263018") or ("5261067") or ("5251208") or ("5229996") or ("5224215") or ("5221867") or ("5220211")).PN.	USPAT
17	IS&R	27	(("5206941") or ("5239562") or ("5237590") or ("5237561") or ("5235597") or ("5210858") or ("5204882") or ("5204856") or ("5204855") or ("5198708") or ("5197142") or ("5195092") or ("5185736") or ("5182749") or ("5179667") or ("5163068") or ("5155393") or ("5151623") or ("5146585") or ("5173899") or ("5172011") or ("5170079") or ("5167031") or ("5163149") or ("5140184")).PN.	USPAT
18	IS&R	16	(("3787665") or ("3773978") or ("3764999") or ("3725593") or ("3723760") or ("3723714") or ("3719832") or ("3729715") or ("3646272") or ("3644895") or ("3644677") or ("3573743") or ("3555194") or ("3603816") or ("3601543")).PN.	USPAT

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•	Time Stamp	Comments	Error Definition	Errors
16	1999/11/23 14:36			0
17	1999/11/23 14:37			0
18	1999/11/23 14:37			0
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	Туре	Hits	Search Text	DBs
19	BRS		((("5379398") or ("5369635") or ("5365228") or ("5363377") or ("5363377") or ("5361260") or ("5357480") or ("5353429") or ("5353281") or ("5345440") or ("5343096") or ("5333299") or ("5333293") or ("5333130") or ("5327466") or ("5327468") or ("5327466") or ("5327425") or ("5327394") or ("53274702") or ("5327394") or ("5327277") or ("5321368") or ("5315181") or ("5315180") or ("5315181") or ("5313462") or ("5287459") or ("5287476") or ("5287459") or ("5287476") or ("5287359") or ("5287476") or ("53134636") or ("5125089") or ("5124980") or ("5125089") or ("5124980") or ("5122693") or ("5121390") or ("5122693") or ("5060241") or ("5060239") or ("5075757") or ("5047725") or ("5047725") or ("5047921") or ("5044747") or ("5043982") or ("5034917") or ("5043982") or ("5034917") or ("50433801") or ("5034917") or ("50433801") or ("5034917") or ("50433801") or ("5034917") or ("50433801") or ("5047755")	USPAT

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	1999/11/23			0
19	14:38			0
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		Issu				Current
	Document ID	_	Pages	Title	Abstract	OR
		Date				
1	US 5987576 A	1999 1116	12	Method and apparatus for generating and distributing clock signals with minimal skew		711/167
2	US 5986943 A	1999 1116	15	Semiconductor memory device for shortening the set up time and hold time of control signals in synchronous DRAM		365/189. 04
3	US 5956290 A	1999 0921	20	DLL circuit and a memory device building the same in		365/233
4	US 5955897 A	1999 0921	9	Signal generation decoder circuit and method		326/105
5	US 5953284 A	1999 0914	39	Method and apparatus for adaptively adjusting the timing of a clock signal used to latch digital signals, and memory device using same		365/233
6	US 5946244 A	1999 0831	19	Delay-locked loop with binary-coupled capacitor		365/194

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		ieval ssif	Inventor	บ	s	С	₽	1	2	3.	4	5
1	-		Johnson, Leith L. , et al.					⊠				
2			Isa, Satoshi						×	☒		
3			Matsuzaki, Yasurou					×	×		☒	
. 4	-		Narayana, Pidugu L. , et al.					⊠				
5			Baker, Russel Jacob , et al.									
, 6			Manning, Troy A.					×	⊠	⊠	⊠	
				فيسييسين	أحسسيين			***************************************	***************************************	*******	******	

		Issu				Current
	Document ID		Pages	Title	Abstract	OR
		Date				
7	US 5940855 A	1999 _. 0817	13	System and method for determining relative cache performance in a computer		711/118
			••••••••••	system		
				Synchronous semiconductor memory device including internal clock signal		
8	US 5940344 A	1999 0817	23	generation circuit that generates an internal clock signal		365/233 ¨
				synchroniz ing in phase with external clock signal at high precision		
9	US 5933623 A	1999 0803	46	high precision Synchronous data transfer system		713/400
10	us 5923613 A	1999 0713	18	Latched type clock synchronizer with additional 180.degreepha se shift clock		365/233 -
11	US 5923611 A	1999 0713	16	Memory having a plurality of external clock signal inputs		365/233
12	US 5920518 A	1999 0706	12	Synchronous clock generator including delay-locked loop		365/233

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	Retrieval Classif	Inventor	U	s	С	P	1	2	3	4	.5
7		Kayes, Kevin W. , et al.							⊠		
8 .		Murai, Yasumitsu , et al.					×	×			
9		Umemura, Masaya , et al.					⊠	☒		⊠	
10 .		Tien, Li-Chin , et al.									
11		Ryan, Kevin J.								☒	
12		Harrison, Ronnie M. , et al.					⊠			⊠	

	Document ID	Issu e Date	Pages	Title	Abstract	Current OR
13	US 5896347 A	1999 0420	25	Semiconductor memory system using a clock-synchrono us semiconductor device and semiconductor memory device for use in the same		365/233
14	US 5886948 A .	1999 0323	16	Memory having a plurality of external clock signal inputs		365/233
15	US 5886946 A	1999 0323	67	Semiconductor memory device allowing reduction in power consumption during standby		365/233
16	US 5870594 A	1999 0209	17	Data transfer system and method		713/500
17	US 5870445 A	1999 0209	6	Frequency independent clock synchronizer		375/371
18	US 5822777 A	1998 1013	17	Dual bus data storage system having an addressable memory with timer controller fault detection of data transfer between the memory and the		711/167

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	Retrieval Classif	Inventor	ט	s	С	P	1	2	3	4	5
13		Tomita, Hiroyoshi , et al.		**************************************		***************************************					
14		Ryan, Kevin J.							×		
15		Ooishi, Tsukasa					×			\boxtimes	
16		Doi, Toshio , et al.					⊠		⊠		
17		Farwell, William D.					☒		⊠		
18]	Leshem, Eli , et al.									

	T	Issu				
	Document ID		Pages	Title	Abstract	Current OR
19	US 5812482 A	1998 0922	8 ·	Wordline wakeup circuit for use in a pulsed wordline design		365/230. 06
20	US 5812462 A	1998 0922	10	Integrated circuit clock input buffer		365/189. 05
				Dynamically configurable memory system having a programmable controller		
21	US 5768560 A	1998 0616	28	including a frequency multiplier to maintain memory timing resolution		711/167
			0	for different bus speeds		
22	US 5767715 A	1998 0616	9	Method and apparatus for generating timing pulses accurately skewed		327/159
	,			relative		,.
23	US 5764091 A	1998 _. 0609	27 ·	to clock Method and system for clock-signal waveform correction		327/175
24	US 5708611 A	1998 0113	36	Synchronous semiconductor memory device		365/195
25	US 5652758 A	1997 0729	9	Data resynchronizati on		370/503
26	US 5652530 A	1997 0729	9	Method and apparatus for reducing clock-data skew by clock shifting		326/93

	Retrieval Classif	Inventor	U	J 8	3 0	E) 1	. 2	2 3	3 4	5
19		Jiang, Yong H. , et al.] [] [] [) 🗵	3 [ם כ	
20		Merritt, Todd A.				ם כ] 🗵] 🗵	ן [] [ם
21 .		Lieberman, Donald A. , et al.	Ŧ				X				
		Marquis, Steven R. , et al.									
23	į.	Sumita, Masaya , et al.					\boxtimes				
24		Iwamoto, Hisashi , et al.					⊠	⊠	Ø	⊠	
25		Donley, Greggory D.					⊠				
		Ashuri, Roni						\boxtimes		⊠	

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	Document ID e Pag		Pages	Title	Abstract	Current OR
27	US 5619157 A	1997 0408	36	Synchronizing circuit with dynamic and static latch circuitry		327/203
28	US 5615358 A	1997 0325	18	Time skewing arrangement for operating memory in synchronism with a data		713/501
29	US 5604884 A	1997 0218	13	processor Burst SRAMS for use with a high speed clock		711/167
30	US 5602878 A	1997 0211	10	Method of delivering stable data across an asynchronous interface		375/354
31	US 5568474 A	1996 1022	18	Ping-pong communication method and apparatus		370/294
32	US 5566108 A	1996 1015	13	Synchronized semiconductor memory		365/233
33	US 5539786 A	1996 0723	6	Digital circuit for generating a clock signal		375/373
34	US 5517459 A	1996 0514	30	Semiconductor memory device in which data are read and written asynchrono usly with application of		365/230. 08

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		Retrieval Classif	Inventor	υ	s	С	P	1	2	3	4	5
:	27		Kumata, Ichiro , et al.					×	×	×		
	28		Vogley, Wilbur C.					×				
,	29 .		Thome, Gary W. , et al.					☒	☒			
	30		Cross, Leonard W.					×				
	31		Wissman, Charles H.									
	32		Kitamura, Mamoru							⊠		
	33 .		Snelgrove, Andrew H.					☒		☒		
•	34		Ooishi, Tsukasa						⊠			

		Issu				
	Document ID		Pages	Title	Abstract	Current OR
		Date				OR
35	US 5440515 A	1995 0808	37	Delay locked loop for detecting the phase difference of two signals having different frequencies		365/194
36	US 5430660 A	1995 0704	22	Digital pulse generator		702/124
37	US 5420814 A	1995 0530	22	Small skew-clocked synchronous semiconductor device		365/189. 11
38	US 5386150 A	1995 0131	26	Tracking pulse generator and RAM with tracking precharge pulse generator		327/141
39	US 5305451 A	1994 0419	11	Single phase clock distribution circuit for providing clock signals to multiple chip integrated circuit systems		713/500
40	US 5305320 A	1994 0419	8	Peripheral communications network	·	370/229
41	US 5252977 A	1993 1012	21	Digital pulse generator using digital slivers and analog vernier		341/182
				increments	······································	

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	Retrieval Classif	Inventor	U	s	С	P	1	2	3	4	5.
35		Çhang, Ray , et al.						\boxtimes		\boxtimes	
36		Lueker, Jonathan , et al.					⊠		Ø	X	⊠
37		Takahashi, Hiroyuki							×		
38		Yonemoto, Ryuji					×	×	⊠		
39		Chao, Hu H. , et al.									
40		Andrews, Michael W. , et al.							⊠	☒	
41		Lueker, Jonathan , et al.									

		Issu				Current
	Document ID	e Date	Pages	Title	Abstract	OR
42	US 5245584 A .		10	Method and apparatus for compensating for bit line delays in semiconduc tor memories		365/233
43	US 5229965 A	1993 0720	11	Serial accessible semiconductor memory device		365/189. 04
44	US 5224129 A	1993 0629	20	Method of synchronizing signals of a pulse generator		375/371
45	US 5208598 A	1993 0504	21	Digital pulse generator using leading and trailing edge placement		341/182
46	US 5146585 A		26	Synchronized fault tolerant clocks for multiprocessor systems		713/400
47	US 5025457 A	1991 0618	23	Synchronizing continuous bit stream oriented terminals in a communicat ions network		375/354
48	US 5023484 A	1991 0611	12	Architecture of high speed synchronous state machine		326/46
49	US 4879481 A	1989 1107	13	Dual I/O macrocell for high speed synchronous state machine		326/46
50	US 4843455 A	1989 0627	12	Color television signal sampling clock phase control system		348/393

	Retrieval	Inventor	ט	s	C	P	1	2	3	4	5
	Classif	Inventor					_			-	
42		Zampaglion e, Michael A. , et al.	i								
43		Inoue, Kazunari									
44		Lueker, Jonathan , et al.						×		×	×
45		Lueker, Jonathan , et al.							×	×	×
46		Smith, III, Thomas B.							×	×	
47		Ahmed, Hassan M.					☒				
48		Pathak, Jagdish , et al.						☒	☒		
49 ·		Pathak, Jagdish , et al.					Ø				
50		Suzuki, Norio					⊠			☒	

		Issu				
	Document ID		Pages	Title	Abstract	Current OR
51	US 4843263 A		8	Clock timing controller for a plurality of LSI chips		327/297
52	US 4736393 A	1988 0405	27	Distributed timing control for a distributed digital communication system		375/356
.53	US 4694291 A	1987 0915	11	Device for transmitting a clock signal accompanied by a synchronization		340/825. 2
54	US 4691302 A	1987 0901	12	signal Circuit arrangement comprising a matrix-shaped memory arrangement for variably adjustable delay of digital signals		365/240
55	us 4682327 A	1987 0721	26	Polyphase phase lock oscillator		370/503
56	US 4680779 A	1987 0714	13	Distributed clock synchronization in a digital data switching system		375/356
57	US 4460983 A	1984 0717	9	Integrated dynamic read-write memory		365/189. 07

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	Retrieval Classif	Inventor	ט	s	С	P	1	2	3	4	5.
51		Ando, Mitsugu					⊠				
52		Grimes, Gary J. , et al.						×			
53 .		Denhez, Alain , et al.					×				
54		Mattausch, Hans J.						⊠			
55 .		Okumura, Yasuyuki , et al.								⊠	
56		Wakerly, John F.									
57		Michael, Ewald					⊠				

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		Issu		·	Current	
	Document ID	e Date	Pages	Title	Abstract	OR
58	US 4419739 A		10	Decentralized generation of synchronized clock control signals having dynamicall		713/600
				y selectable periods		
59	US 4309673 A	1982 0105	14	Delay lock loop modulator and demodulator		332/112
60	US 4229816 A	1980 1021		Timing signal generation and distribution system for TDM telecommun ications		370/216
61	US 4138694 A	1979 0206	27	Video signal recorder/reprod ucer for recording and reproducing pulse		386/91
	US 3947829	1976	••••••	signals	•••••••••••••••••••••••••••••••••••••••	
62	A 394/829	0330	14	Logical circuit apparatus		365/233
63	US 3859466 A	1975 0107	1.0	RECIPROCAL SYNCHRONIZATION OF OSCILLATORS OF A TIME MULTIPLEX TELEPHONE		370/507
				COMMUNICAT ION NETWORK		
64	US 3810385 A	1974 0514	6	TRANSDUCER MEANS FOR ULTRASONIC EXTENSOMETER		73/629
65	US 3723714 A	1973 0327	6	DIGITAL PHASE TRACKER		327/159 ⁻
66	US 3432816 A	1969 0311	23	TEXT NOT AVAILABLE		365/76
67	US 3413615 A	1968 1126	4	TEXT NOT AVAILABLE		365/77

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	Retrieval Classif	Inventor	ט	s	С	P	1	2	3	4	-5
58	·	Blum, Arnold									
59		Norberg, Gayle R. , et al.					Ø	×	⊠	Ø	
60		Breidenste in, Charles J. , et al.							⊠		
61		Doi, Toshitada , et al.					⊠				
62 .		Suzuki, Yasoji				☒	⊠	☒	Ø		
63		Hartmann, Lothar						⊠	×		
64	F	McFaul, Howard J., et al.									⊠
65 .	ŀ	Jackson, Harold W. et al.						☒		☒	
66							Ø			Ø	
67		·					☒				

	Document ID	Issu e Date	Pages	Title	Abstract	Current OR
68	US 3064241 A	1962 1113	12	TEXT NOT AVAILABLE		365/77

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Retrieval Classif	Inventor	ט	S	,C	P	1	2	3	.4
68 .						×	⊠	☒	☒